REMARKS/ARGUMENTS

Claims 1-51 were presented for examination. Claims 37-51 were withdrawn from considerations leaving claims 1-36 pending in this application. In an Official Office Action dated June 28, 2005, claims 1-36 were rejected. The Applicants thank the Examiner for examination of the claims pending in this application and address the Examiner's comments below.

35 U.S.C. §103(a) Obviousness Rejection of Claims

Claims 1-36 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,633,945 ("Fu et al.") in view of U.S. Patent No. 6,295,571 ("Scardamalia") and further in view of U.S. Patent No. 5,915,104 ("Miller"). The Applicants respectively traverse these rejections in light of the following remarks and respectfully request reconsideration.

MPEP §2143 provides:

> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teaching. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

Claim 1 states, among other things, "at least one memory module slot coupled to said memory module and in direct communication with said peripheral bus." With respect to claim 1, the Examiner admits that Fu et al. "does not explicitly disclose ... that the memory module slot is in direct communication with said peripheral bus." See USPTO communication dated 6/28/05, pp. 2-3. The

Examiner asserts that this missing element is found in Miller. The Applicants respectfully disagree with the Examiner's conclusion.

Miller appears to teach or suggest "a mechanism in a computer system for minimizing memory latencies". Miller Abstract. Miller continues by stating, "An improved high-speed packet switched router is used to route packets quickly and efficiently between the microprocessor and the main memory. The computer system also supports PCI devices by implementing a bridge which acts as an interface between a PCI bus and the packet switched router." Miller, Col. 2, lines 57-63. The mechanism taught by Miller and the Applicants' invention are distinct.

Figure 1 of Miller, upon which the Examiner relies, appears to show computer memory DRAM (item 104) in communication with a memory bus (item 105) which is in turn in communication with a memory controller (item 102) which is in turn in communication with a switched router (item 101) which is in turn in communication with a bridge (item 110 and 114). Figure 2 of Miller seems to teach that the Bridge includes a PCI/GIO Bus (item 201). See Miller Figures 1 and 2. Miller does not teach or suggest a memory module slot coupled to a memory module that is in direct communication with a peripheral bus as cited in claim 1. In fact Miller states, "the Bridge ASIC connects the PCI bus to the system bus. The system bus then connects to main memory." Miller, Col. 9, lines 12-4. Both in text and depicted in the figures, Miller appears to teach and suggest the existence of several intermediary components such as a memory controller, switched router, and system bus, between memory and a peripheral bus.

The Examiner seems to focus on Miller's statement with regard to latency in which Miller states, "this means that the latency to main memory is longer than it is in a computer whereby the PCI bus is [sic] directly connects to main memory." Miller, Col. 9, lines 14-16. The statement however is taken out of

context. A more telling reading can be realized by considering the surrounding sentences. The section states, " As described above, the Bridge ASIC connects the PCI bus to the system bus, the system bus then connects to main memory. This means that the latency to main memory is longer than in a computer whereby the PCI bus is [sic] directly connects to main memory. By not connecting the PCI bus directly to the main memory, a computer can have multiple PCI busses, and the total I/O bandwidth of the system is not limited to the bandwidth of a single PCI bus." Miller Col. 9. lines 11-20. (emphasis added)

The Applicant's invention and Miller appear to be solving similar problems but using different and distinct approaches. The Applicants claim a system having, among other things, a "memory module slot coupled to said memory module bus and in direct communication with said peripheral bus." Miller however appears to address increased memory latency caused by having multiple PCI busses by placing a memory controller and a packet switched router between memory and the PCI busses. Miller does not teach or suggest a memory module slot in direct communication with a peripheral bus, and in fact appears to teach away from the Applicants' invention.

To establish a prima facie case of obviousness, the prior art must teach or suggest all the claim limitations. Fu et al. in view of Scardamalia in further view of Miller does not teach or suggest an at least one memory module slot coupled to a memory module and in direct communication with a peripheral bus as stated in claim 1. Accordingly, the Applicants submit that claim 1 is patentable over Fu et al. in view of Scardamalia in further view of Miller and respectfully request the Examiner withdraw the rejection.

Claims 2-12 depend from claim 1 and, as the prior art must teach or suggest all of the combined limitations found in the combined claims, the Applicants submit, for at least the aforementioned reasons, that claims 2-12 are

patentable over Fu et al. in view of Scardamalia in further view of Miller. The Applicants respectfully request reconsideration.

With respect to claim 13, the Examiner's reliance on Fu et al. is without foundation. The Examiner asserts that Fu et al. teaches or suggests "at least one memory module slot coupled to said memory module bus (1300, fig.2, col. 3, lines 41-45; memory modules slots allow plurality if DIMM chips to be coupled)." USPTO Communication pp. 3-4. Claim 13 however states, among other things, "at least one memory module slot coupled to said memory module bus and in direct communication with said graphics bus." (emphasis added) The Examiner fails to identify where Fu et al. teaches or suggests "at least one memory module slot ... in direct communication with said graphics bus." The cited figure appears to show memory units in communication with memory control units which are in turn in communication with a flow control unit. Neither Figure 2, nor the text cited, appears to teach or suggest a memory module slot in direct communication with a graphics bus.

For a rejection to stand under 35 U.S.C. §103, the cited prior art or references must teach or suggest all of the limitations of the claim. Fu et al. in view of Scardamalia fails to teach or suggest a memory module slot in direct communication with a graphics bus. Accordingly, the Applicants submit that claim 13 is patentable over Fu et al. in view of Scardamalia and respectfully request the rejection be withdrawn. As claims 14-24 depend on claim 13, the Applicants assert claims 14-24 are patentable for at least the reasons mentioned above and respectfully request reconsideration.

With respect to claim 25, the Examiner admits that Fu et al. in view of Scardamalia fails to teach coupling a processor to a system maintenance control block and a memory block. See USPTO Communication, pg. 7. The Examiner offers no additional art to compensate for this weakness of Fu et al. and Scardamalia. Instead the Examiner states that such an introduction would be

obvious to one of ordinary skill. The Applicants reject such a conclusion. The very lack of such a coupling strengthens the Applicants' position that their invention is indeed novel and is not obvious. As the Examiner has failed to identify prior art, either singularly or in combination that teaches or suggests all of the claimed elements, the rejection must fail. Accordingly, the Applicants respectfully request that the rejection be withdrawn. As claims 26-36 depend on claim 25, the Applicants assert they are patentable over Fu et al. in view of Scardamalia for at least the same reasons and request their rejections be withdrawn.

In view of all of the above, the claims are now believed to be allowable and the case in condition for allowance which action is respectfully requested. Should the Examiner be of the opinion that a telephone conference would expedite the prosecution of this case, the Examiner is requested to contact Applicants' attorney at the telephone number listed below.

No fee is believed due for this submittal. However, any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

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